Features

• 200pin, unbuffered small outline dual in-line memory module (SODIMM)
• Fast data transfer rates: PC-2100, PC-2700, PC3-3200
• Single or Dual rank
• 256MB(32Megx64), 512MB (64Meg x 64), 1GB(128 Meg x 64)
• JEDEC standard 2.5V I/O (SSTL_2 compatible)
• V_{DD} = V_{DDQ} = 2.5V ±0.1V
• V_{DDSPD} = 2.3V to 3.6V
• Internal, pipelined double data rate (DDR) 2*n*-prefetch architecture
• Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
• Differential clock inputs (CK and CK#)
• Multiple internal device banks for concurrent operation
• Single or Dual rank
• Selectable burst lengths (BL) 2, 4, or 8
• Auto precharge option
• Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
• Serial presence-detect (SPD) with EEPROM
• Selectable CAS latency (CL) for maximum compatibility
• Gold edge contacts
• Pb-free

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP512MBSDU266O01(2)	512MB (64Mx64) 64Mx8 1Rank	PC-2100	DDR-266	2.5-3-3
SP512MBSDU333O01(2)		PC-2700	DDR-333	2.5-3-3
SP512MBSDU400O01(2)		PC-3200	DDR-400	3-3-3
SP001GBSDU266O01(2)	1GB (64Mx64) 128Mx8 2Ranks	PC-2100	DDR-266	2.5-3-3
SP001G BSDU333O01(2)		PC-2700	DDR-333	2.5-3-3
SP001G BSDU400O01(2)		PC-3200	DDR-400	3-3-3

Note:

1. This document supports all SDU Series DDR 200Pin SODIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP512MBSDU266O02-XX

Pin Assignments

200-Pin SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42
3	VSS	53	DQ19	103	VSS	153	DQ43
5	DQ0	55	DQ24	105	A7	155	VDD
7	DQ1	57	VDD	107	A5	157	VDD
9	VDD	59	DQ25	109	A3	159	VSS
11	DQS0	61	DQS3	111	A1	161	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48
15	VSS	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6
21	VDD	71	NC	121	S0#	171	DQ50
23	DQ9	73	NC	123	NC	173	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
27	VSS	77	NC	127	DQ32	177	DQ56
29	DQ10	79	NC	129	DQ33	179	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57
33	VDD	83	NC	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
39	VSS	89	NC	139	DQ35	189	DQ59
41	DQ16	91	NC	141	DQ40	191	VDD
43	DQ17	93	VDD	143	VDD	193	SDA
45	VDD	95	NC	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	VDDSPD
49	DQ18	99	A12	149	VSS	199	NC

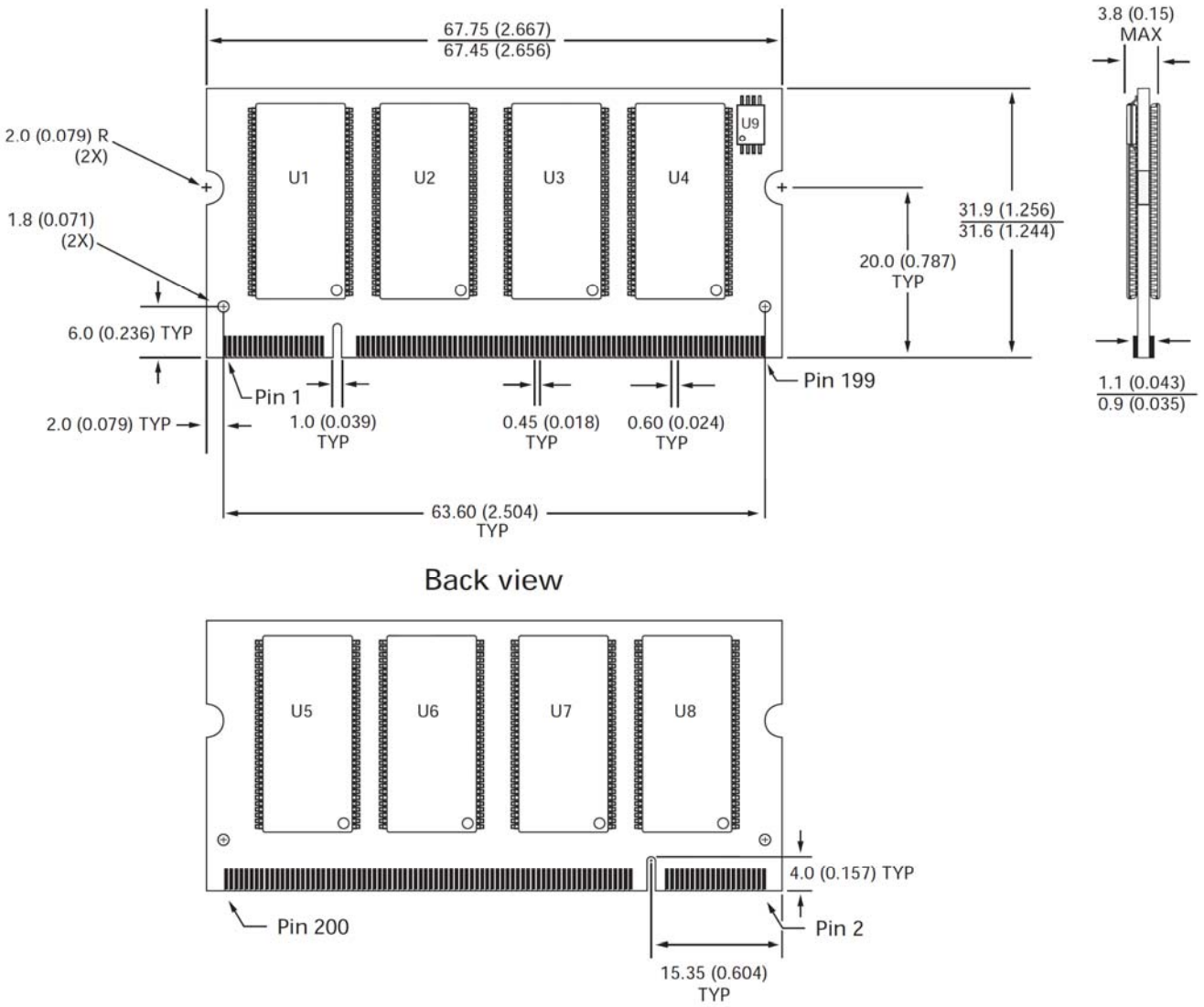
200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VREF	52	VSS	102	A8	152	DQ46
4	VSS	54	DQ23	104	VSS	154	DQ47
6	DQ4	56	DQ28	106	A6	156	VDD
8	DQ5	58	VDD	108	A4	158	CK1#
10	VDD	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	VSS
14	DQ6	64	VSS	114	VDD	164	DQ52
16	VSS	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	VDD
20	DQ12	70	VDD	120	CAS#	170	DM6
22	VDD	72	NC	122	NC	172	DQ54
24	DQ13	74	NC	124	NC	174	VSS
26	DM1	76	VSS	126	VSS	176	DQ55
28	VSS	78	NC	128	DQ36	178	DQ60
30	DQ14	80	NC	130	DQ37	180	VDD
32	DQ15	82	VDD	132	VDD	182	DQ61
34	VDD	84	NC	134	DM4	184	DM7
36	VDD	86	NC	136	DQ38	186	VSS
38	VSS	88	VSS	138	VSS	188	DQ62
40	VSS	90	VSS	140	DQ39	190	DQ63
42	DQ20	92	VDD	142	DQ44	192	VDD
44	DQ21	94	VDD	144	VDD	194	SA0
46	VDD	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	VSS	200	NC

Pin Description

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
BA0–BA1	Input	**Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0 ,CKE1	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates the internal clock, input buffers, and output drivers.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#, S1#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect devices.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
DM0–DM7	I/O	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
DQ0–DQ63	I/O	**Data input/output:** Bidirectional data bus.
DQS0–DQS7,	I/O	**Data strobe:** Output with read data, input with write data. DQS is edge aligned with read data, center-aligned with write data. Used to capture data.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 2.5V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +2.3V to +3.6V.
V_{REF}	Supply	SSTL_2 reference voltage. ($V_{DD}/2$)
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Simplified Mechanical Drawing(x8 1Rank)

X64 DIMM, populated as one physical rank of x8 DDR SDRAMs

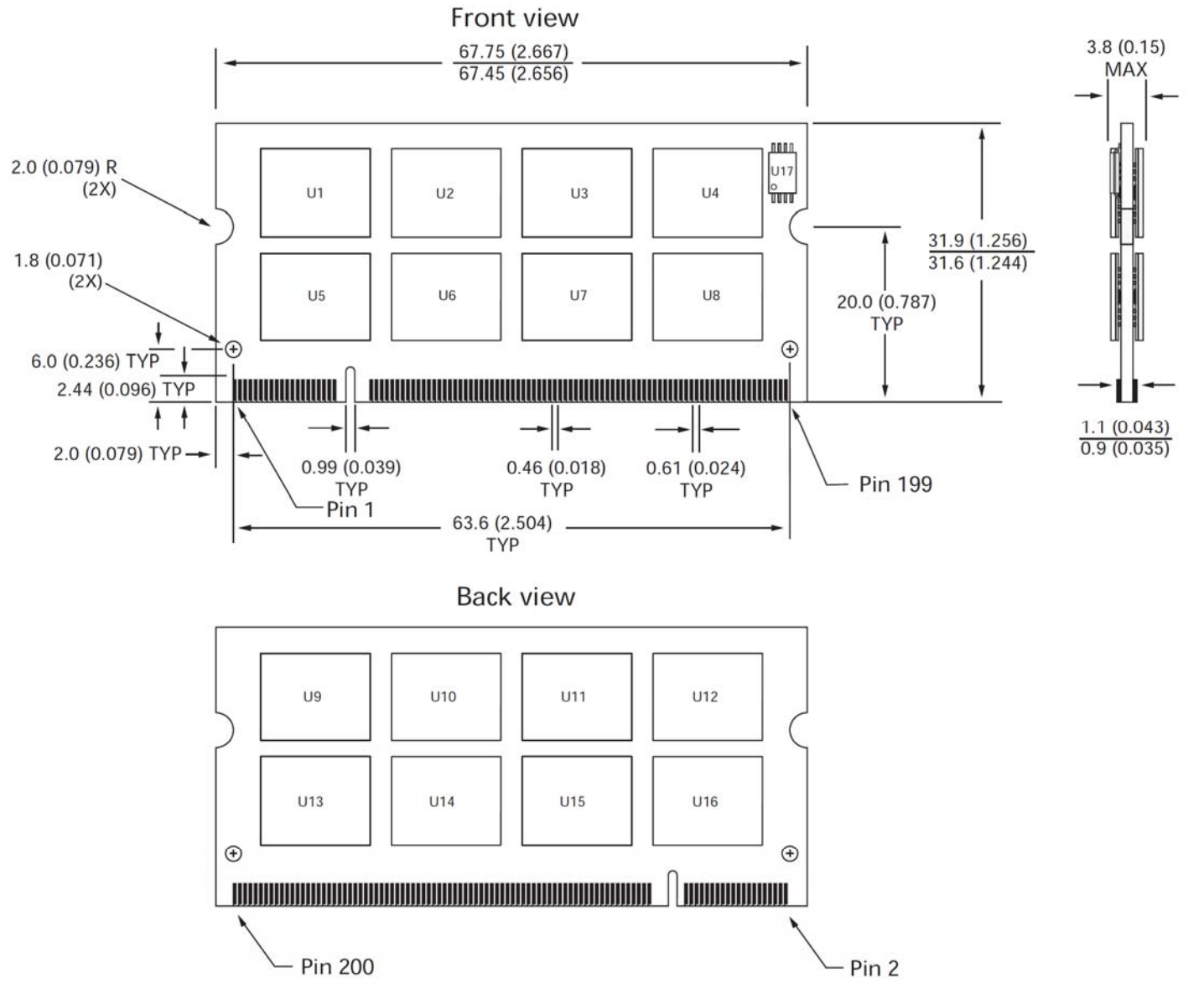


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks)

X64 DIMM, populated as two physical ranks of x8 DDR SDRAMs



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.